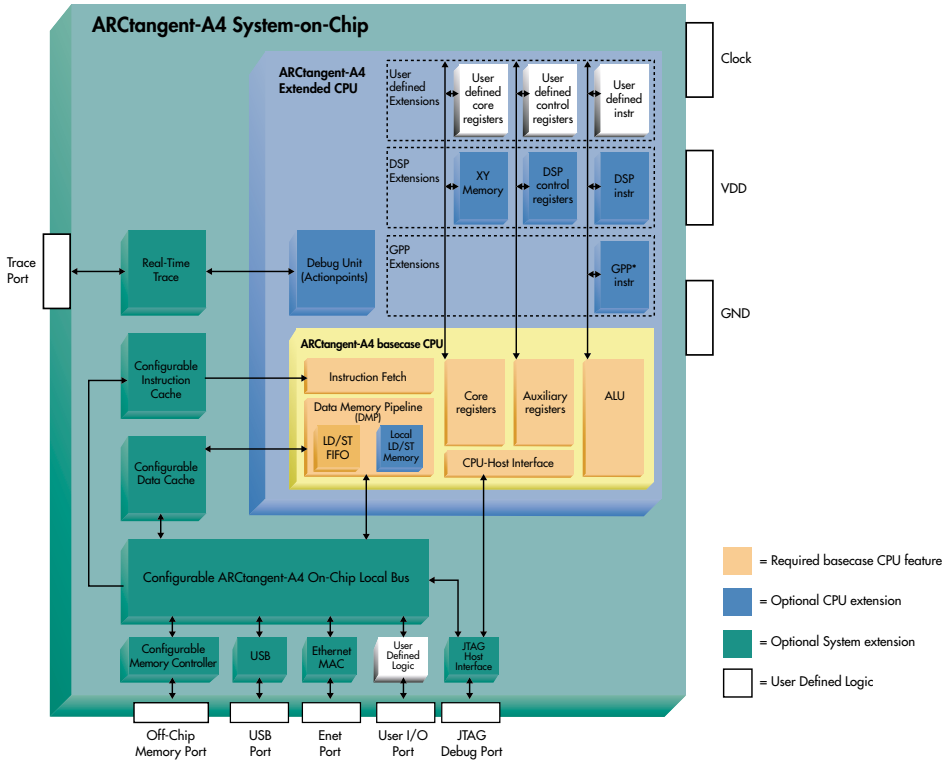
The ARCtangent™-A4 Processor

Introduction

The ARCtangent-A4 microprocessor is a 32-bit user-customizable RISC core for ASIC, system-on-chip (SoC), ASSP, and FPGA development. It is synthesizable, configurable, and extendible—developers can modify and extend the architecture for specific applications. This flexibility allows developers to creatively tailor the hardware for the application, instead of bending the system to fit a rigid CPU architecture. Developers can optimize the ARCtangent-A4 processor for various criteria, including computational performance, signal processing, I/O throughput, power consumption, silicon area, and cost.

As a synthesizable core delivered in HDL, the ARCtangent-A4 processor is portable to almost any manufacturing process, synthesis library, and foundry. ARC International customers are using the core in a variety of applications, including disk-drive controllers, digital cameras, broadband modems, cordless phones, Bluetooth™ wireless-technology devices, audio/video codecs, encryption chips, and network routers. The ARCtangent-A4 processor is compatible with existing design flows and comes with easy-to-use development tools, including the ARChitect™ configuration tool, which has a point-and-click user interface for modifying the processor.

At the heart of the ARCtangent-A4 processor is a 32-bit RISC architecture with a four-stage instruction pipeline. The instruction set is orthogonal, with all data-addressing modes implemented for all arithmetic and logical instructions. Most instructions have optional conditional (predicated) execution. The instruction set, register file, condition codes, caches, buses, and other architectural features are user-configurable and extendable. Thanks to multiple CPU I/O interfaces and a low gate count, the ARCtangent-A4 processor lends itself to multiprocessor designs. Some ARC International customers have integrated dozens of cores on a single chip.



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ARCtangent-A4 Processor Feature List

CPU Architecture

- Harvard or von Neumann bus architecture
- Four-stage instruction pipeline
- 32-bit data bus and address buses
- 24-bit instruction fetch address bus
- Configurable instruction cache (1-, 2-, or 4-way, 0-31 kB)
- Configurable writeback data cache (1-, 2-, or 4-way, 0-31 kB)
- Optional on on-chip load/store RAM
- Optional 32-bit timer(s)

Instruction Set Architecture (ISA)

- 30 standard instructions (base-case core)
- Up to 70 additional extension instruction codes available
- Single-cycle instructions
- Zero-overhead loops
- Conditional ALU instructions
- Single-cycle immediate data
- Jumps/branches with single-instruction delay slot
- Multiple delay-slot execution modes

Registers

- 36 x 32-bit core register file (base-case core)
- Optional 28 x 32-bit extension core registers
- Optional 2^{32} x 32-bit auxiliary registers (single-cycle access)

Data-Memory Pipeline

- Configurable data cache
- Load/store queue
- Configurable load/store RAM
- Peripheral interface block
- AMBA AHB slave interface

Optional Extension Instructions

- 32-bit barrel shifter/rotate block
- 32 x 32-bit multiplier (choice of two versions)
- MIN/MAX instructions
- NORMalize (find first bit) instruction
- SWAP instruction

Optional DSP Extensions

- 16 x 16-bit multiply-accumulate (MAC) instruction
- 24 x 24-bit MAC instruction
- Dual 16 x 16-bit MAC instruction
- 32-bit signed saturating ADD/SUB instructions
- Configurable banks of XY memory for DSP data
- Modulo and bit-reverse addressing
- Variable-offset pre- and post-increment addressing modes
- Zero-overhead loops and branches
- Optimized DSP software function library

Power Management

- Sleep mode
- Clock Gating Option and on-chip RAM controls

Interrupts and Exceptions

- 16 interrupt sources (extendable to 32)
- Software interrupt instruction (SWI)
- Configurable priority levels

Host Interface/Debug Features

- Non-intrusive on-chip debug system
- JTAG or parallel port
- Start, stop, single step via special registers
- Access to register set and CPU memory
- Breakpoint instruction
- Optional Real-Time Trace module

System Options

- USB 1.1 Host/Device controller
- Up to eight 10/100Mbps Ethernet MACs
- Up to eight UARTs
- AMBA AHB master interface

ISA Overview

The ARCtangent-A4 microprocessor core has 16 base-case instructions with 14 variations to provide a set of 30 arithmetic/logical, load/store, and branch/jump instructions. Developers may define up to 16 additional dual-operand and 54 additional single-operand instructions for application-specific purposes.

Core Registers

The ARCtangent-A4 processor can accommodate up to 64 core registers. The base case processor has 36 core registers, 29 are used as general purpose registers and the rest are used for link, loop and data indicator registers.

DSP Extensions

Using ARChitect™, the developer can boost the computational performance of the processor by adding multiply and accumulate instructions, arithmetic instructions and on-chip XY memory with integrated programmable address generation logic for fast data access.

Auxiliary Registers

The auxiliary register set is an additional memory space accessed using dedicated load/store instructions, hence auxiliary register access does not contend with real memory access. The auxiliary register space is comparable to an I/O register space because it may contain configuration registers that would normally be memory-mapped or occupy core register slots. Auxiliary registers have a 32-bit address bus, 32-bit data and can be accessed in a single cycle by the dedicated load/store instructions. The ARCtangent-A4 processor reserves a range of registers for use as status and control registers but this still leaves a huge range of available addresses (~4 billion) for user extensions.

Multiple I/O Interfaces

In addition to supporting conventional I/O transactions through the auxiliary registers and load/store bus, the ARCtangent-A4 processor also opens up the interfaces to the core register set, ALU, and condition-code unit. This allows developers to easily control the application flow, and provides fast and direct access to extension functions. Developers can choose the optimal connection according to the bandwidth and latency required. The interfaces support multiple concurrent I/O transactions.

Developers can also add third-party and legacy IP to the ARCtangent-A4 processor using AMBA AHB interfaces. Two types of interfaces are supplied: master and slave. The slave interface connects to the data-memory pipeline and can read data in parallel with main-memory accesses, further reducing bus contention. The master interface connects through the main-memory system and allows burst accesses to and from main memory.

Condition Codes

The ARCtangent-A4 processor has 32 possible condition codes. The base-case processor defines the first 16 codes (00-0F). The remaining 16 codes (10-1F) are available for user extensions. Developers may use them to define additional tests on the internal condition flags, to test extension status flags from external sources, and to test combinations of external and internal flags. Most base-case and extension instructions can execute conditionally on the status of all base-case and extended condition codes.

Software Development Tools

The ARCtangent series of processors is supported by the MetaDeveloper™ tool suite. This includes the MetaWare® C/C++ compiler, assembler, linker, profiler and the SeeCode™ debugger.

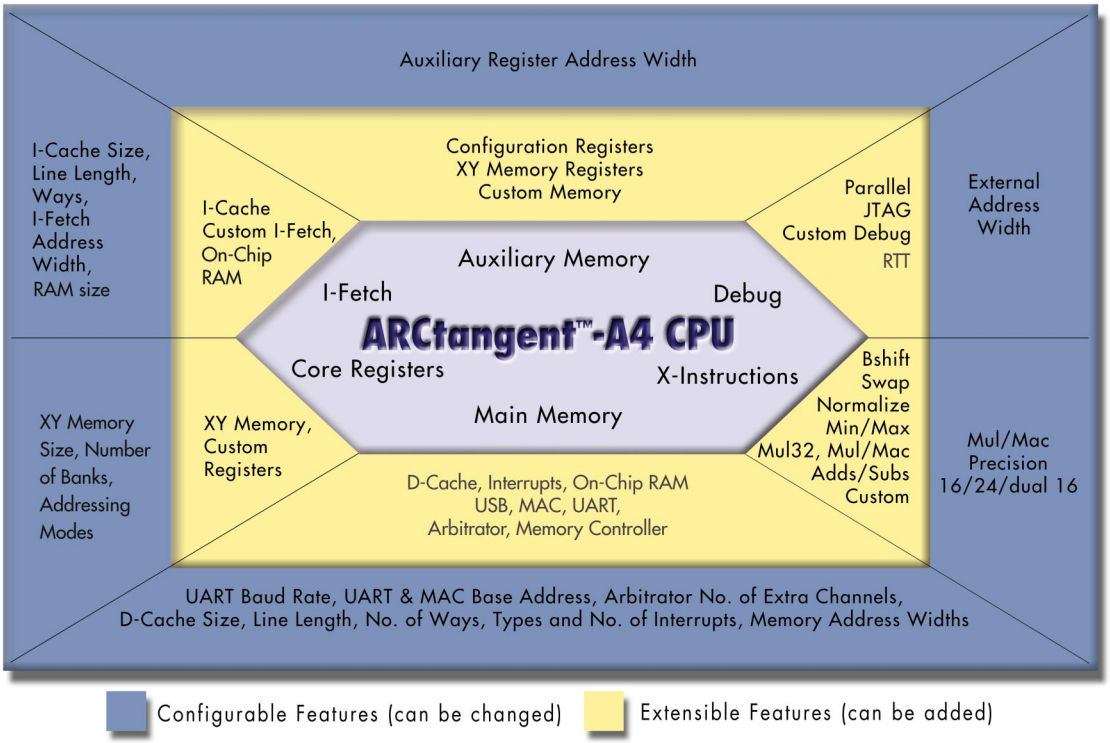
The software tool developers have worked closely with the processor design team to ensure that the toolchain has been highly optimized for the ARCtangent family of processors. The tool chain fully supports the capabilities of the ARCtangent processor including multiprocessor debugging and extensibility for processor customizations. The IDE shipped with the tools includes a sophisticated, configurable editor that can emulate popular editors such as "VI".

Software IP

ARC International's powerful, royalty-free Precise/MQX™ RTOS is delivered with source code; it has a modular architecture to provide complete control over code footprint and feature set. ARC International also offers pre-integrated embedded middleware and protocol stacks. These are designed in a modular and efficient manner to offer the developer the power and flexibility that they require. Examples of the protocols supported include: TCP/IP, HTTP, POP3, SMTP, NAT, OSPF and IPSec.

Peripheral IP

The ARChitect tool supports the ability to integrate 10/100Mbps Ethernet Media Access Controllers (MAC), UARTs and USB 1.1 peripherals. The USB 1.1 peripheral supports both Full and Low speed operation and is available in Device only and Host/Device configurations. Each peripheral comes complete with Device drivers to facilitate software integration.



The ARCtangent™-A4 User-Customizable Microprocessor

Development Board

The ARCangel™ is an FPGA based flexible development board that fully supports the configurability and extensibility of the ARCtangent processor. At the heart of the ARCangel development board is a Virtex™-XCV200E FPGA; the ARChitect™ processor configuration tool can target HDL builds at this device so that developers can generate and test their processor configurations at MHz speeds. The FPGA has plenty of spare capacity for custom logic, or even more than one processor. The ARCangel also carries transceivers for peripheral IP so developers can verify their hardware solutions and software performance.

Performance

- Clock frequency (0.18µm): 200MHz
- Clock frequency (0.13µm): 260MHz
- Silicon area (0.18µm): 0.18mm^2
- Silicon area (0.13µm): 0.1mm^2

Figures were generated using typical 0.18µm and 0.13µm under worst case commercial conditions. Note that actual figures depend on the characteristics of a particular technology, operating parameters, processor configuration and synthesis constraints.

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